TITLE OF THE INVENTION

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND STANDARD CELL PLACEMENT DESIGN METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2001-331294, filed October 29, 2001, the entire contents of which are incorporated herein by reference.

Pat. 6,732,344

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor integrated circuit device and a standard cell placement design method and more specifically to the placement of substrate contacts of a standard cell array.

2. Description of the Related Art

In designing standard cell-based LSIs, standard cells, which have previously been standard-designed, are placed through the use of CAD (computer aided design) or EDA (electronic design automation) tools. By suitably forming interconnect lines on the cell array to combine standard cells, any desired circuit can be constructed.

FIGS. 1A and 1B are plan views of conventional standard cell placement patterns.

A standard cell 50a shown in FIG. 1A has a pattern 51 of active regions of a PMOS transistor, a pattern 52